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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,093	09/12/2003	Jeffrey D. Gilbert	42P17020	8868

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EXAMINER	
CHERY, MARDOCHEE	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 10/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 10/662,093	**Applicant(s)** GILBERT ET AL.	
	Examiner Mardochee Chery	**Art Unit** 2188	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 21 September 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: 1-33.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER

Continuation of 11. does NOT place the application in condition for allowance because: 1. Applicants argue on page 10 of the remarks that the combination of Arimilli and WO does not teach or suggest "a cache containing a cache line with a first cache coherency state when accessed from said first interface and a second cache coherency state when accessed from said second interface". Applicant further argue on page 11, paragraph 1 of the remarks that "although Fig. 1 of the WO reference shows that two coherency states may be associated with a cache line, the cited portion of the WO reference does not discloses that a first cache coherency state is associated with accesses from the first interface and a second cache coherency state is associated with accesses from the second interface".
Examiner respectfully disagrees with such assertion. Fig. 1 of WO clearly shows a cache (CS) accessible by a plurality of processors (EPs) through a first interface (BS1) on one side and accessible by additional cache memories, main memory (MEM), or all types of I/O through a second interface (BS2). If a line was recently cached from main memory (MEM) through BS2, said cache line is in the exclusive state, and if one of the processors (EPs) wants to read the cache line, and performs some operation that require changing the state of the cache to modified, another associated processor (EP) trying to read the same cache line through interface BS1 would find it in a modified state; See Fig. 1, p. 6 et seq.
In addition to that, WO clearly discloses that "the state of a cache block may be altered by a particular assigned processor (EP) via a read and write procedure (through interface BS1); the state may also be altered by an internal system query, also known as snooping; it may also be altered by external logic units (through interface BS2), e.g., another individual processor or a second level cache memory, i.e., through external snooping; p. 2, par. 5 to p. 3, par. 1 et seq.", as shown in the processor system of Fig. 1 which is "constructed hierarchically with lower hierarchy stages situated in the direction of first bus BS1 and higher hierarchy stages situated in the direction of second bus BS2; p. 6, par. 4 et seq.". Furthermore, WO discloses "requests can be made between the additional cache memories CS and the individual processors EP (through interface BS1 processors EP guarantee access of a cache line with a first coherency state), and requests between additional cache memories CS and the main memory (through cache memory bus BS2 guarantee accessing a cache line with a second coherency state); p.7, par. 4.
Still further WO discloses "if an SLC has requested an entry of the TLC using the command RDE or RDM and then modified it, it has to ensure that the modified entry is written back in the TLC using the WR command...after the modification of the requested entry (through BS2, See Fig. 1) the requesting SLC may maintain the entry in modified form and identify is as such. It may also write back the entry and, and as a result of writing back (to main memory MEM or TLC through BS2) downgrade the state of the entry and only still put it in the state E...If the cache memory block is requested by an individual processor EP (through BS1, See Fig. 1) situated in a lower hierarchy, the TLC knows that the cache memory block has been changed..."; See p. 11 et seq..

2. Applicants argue on page 12, paragraph 1 of the remarks that "there is no showing by the cited portions of the WO reference of transitions from a single MESI coherency state (e.g., M or E) to a joint coherency state (e.g., MI), as allegedly recited by the claim.
In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., transitions from a single MESI coherency state (e.g., M or E) to a joint coherency state (e.g., MI)) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

3. Applicants argue on page 12, paragraph 2 of the remarks that "there is no showing in Fig. 3 or page 15, ll 15-19 of the WO reference of the limitation of transitioning a second cache coherency state to a third cache coherency state. Fig. 3 only shows transitions between joint cache states (EM, MI, ES, etc.)".
Examiner totally disagrees. As already acknowledged and recognized by Applicants, "Fig. 3 shows transitions between joint cache states (EM, MI, ES, etc.)" and Fig. 3 further shows transitioning from a first, second, third and multiple cache states. Therefore, the claimed invention is clearly made obvious in view of Fig. 3 of the WO reference since Fig. 3 shows transitioning from a first cache coherency state to a second cache coherency state, to a third cache coherency state, etc...Examiner would like to further emphasize that the claims do not distinguish whether said transition is between a single coherency state, a joint coherency, or else. The claims simply recite, "transitioning a second cache coherency state to a third cache coherency state" and as such is not patentable over Fig. 3 of the WO reference.